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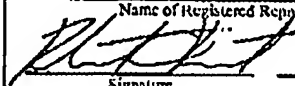
PATENT
5500-68500/TT4418

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/061,671
Filed: February 1, 2002
Inventor:
Michael A. Filippo

Examiner: Wang, Albert C.
Group/Art Unit: 2115
Atty. Dkt. No: 5500-68500

Title: Apparatus and Method for
Selective Clock Control to
Reduce Power Consumption
in an Integrated Circuit

**** CERTIFICATE OF FACSIMILE ****	
TRANSMISSION	
I hereby certify that this paper is being facsimile transmitted to the U.S. Patent and Trademark Office at (571) 273-8300 on the date shown below:	
Robert C. Kowert	
Name of Registered Representative	
	July 29, 2005
Signature	Date

SUPPLEMENTAL AMENDMENT

Mail Stop AP
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Please enter the following amendment in the above-captioned case.

Please amend the case as listed below.

10/061,671 (5500-68500/TT4418)

Meyertons, Hood, Kivlin, Kowert & Goretz, P.C.